# Advances in Carbon Nanotube Technologies: From Transistors to a RISC-V Microprocessor

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## ABSTRACT

Carbon nanotube (CNT) field-effect transistors (CNFETs) promise to improve the energy efficiency of very-large-scale integrated (VLSI) systems. However, multiple challenges have prevented VLSI CNFET circuits from being realized, including inherent nano-scale material defects, robust processing for yielding complementary CNFETs (i.e., CNT CMOS: including both PMOS and NMOS CNFETs), and major CNT variations. In this talk, we summarize techniques that we have recently developed to overcome these outstanding challenges, enabling VLSI CNFET circuits to be experimentally realized today using standard VLSI processing and design flows. Leveraging these techniques, we demonstrate the most complex CNFET circuits and systems to-date, including a three-dimensional (3D) imaging system comprising CNFETs fabricated directly on top of a silicon imager, CNT CMOS analog and mixed-signal circuits, 1 kilobit CNFET static random-access memory (SRAM) memory arrays, and a 16-bit RISC-V microprocessor built entirely out of CNFETs.

## CCS Concepts/ACM Classifiers

• Hardware~Emerging technologies~Circuit substrates~Carbon based electronics; Hardware~Very large-scale integration design~3D integrated circuits

## Author Keywords

Carbon nanotube (CNT) field-effect transistor (CNFET), nanotechnology, very-large-scale integration

## BIOGRAPHY

Gage Hills is currently a post-doctoral researcher at MIT, and will be starting as an assistant professor at Harvard SEAS in July 2021. His research focuses in the area of emerging nano-design, which aims to develop future generations of energy-efficient computing systems, by combining new technology advances in nanomaterials, devices, computing architectures, systems, and integration.


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